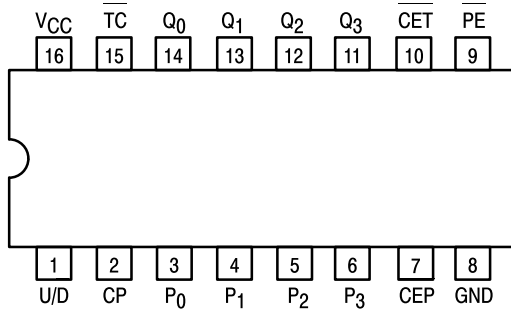**MOTOROLA**

BCD DECADE/MODULO 16 BINARY SYNCHRONOUS BI-DIRECTIONAL COUNTERS

The SN54/74LS168 and SN54/74LS169 are fully synchronous 4-stage up/down counters featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. The SN54/74LS168 counts in a BCD decade (8, 4, 2, 1) sequence, while the SN54/74LS169 operates in a Modulo 16 binary sequence. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

- Low Power Dissipation 100 mW Typical
- High-Speed Count Frequency 30 MHz Typical
- Fully Synchronous Operation
- Full Carry Lookahead for Easy Cascading
- Single Up/Down Control Input
- Positive Edge-Trigger Operation
- Input Clamp Diodes Limit High-Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS168
SN54/74LS169

BCD DECADE/MODULO 16 BINARY SYNCHRONOUS BI-DIRECTIONAL COUNTERS

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 620-09
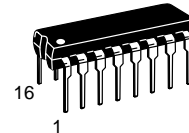
N SUFFIX
PLASTIC
CASE 648-08
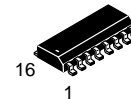
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ   Ceramic
SN74LSXXXN   Plastic
SN74LSXXXD   SOIC

PIN NAMES

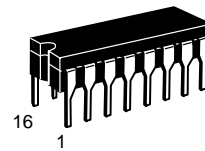|		LOADING (Note a)	
		HIGH	LOW
$\overline{CEP}$	Count Enable Parallel (Active LOW) Input	0.5 U.L.	0.25 U.L.
CET	Count Enable Trickle (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{CP}$	Clock Pulse (Active positive going edge) Input	0.5 U.L.	0.25 U.L.
PE	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
U/D	Up-Down Count Control Input	0.5 U.L.	0.25 U.L.
P_0–P_3	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_0–Q_3	Flip-Flop Outputs	10 U.L.	5 (2.5) U.L.
TC	Terminal Count (Active LOW) Output	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
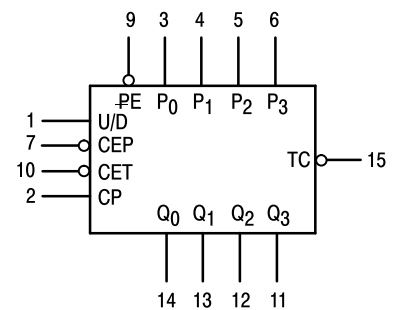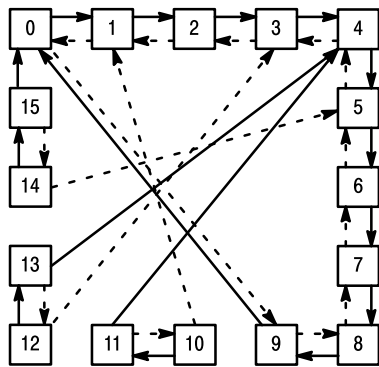b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL

V_{CC} = PIN 16
GND = PIN 8

SN54/74LS168 • SN54/74LS169

STATE DIAGRAMS

SN54/74LS168
UP/DOWN DECADE COUNTER

→ Count Up
- -► Count Down

SN54/74LS169

SN54/74LS168

UP: $TC = Q_0 \cdot Q_3 \cdot (U/\overline{D})$
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{(U/\overline{D})}$
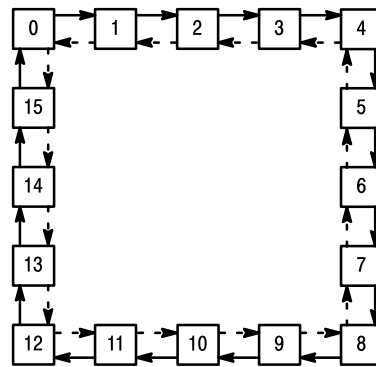
SN54/74LS169

UP: $TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/\overline{D})$
DOWN: $TC = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{(U/\overline{D})}$
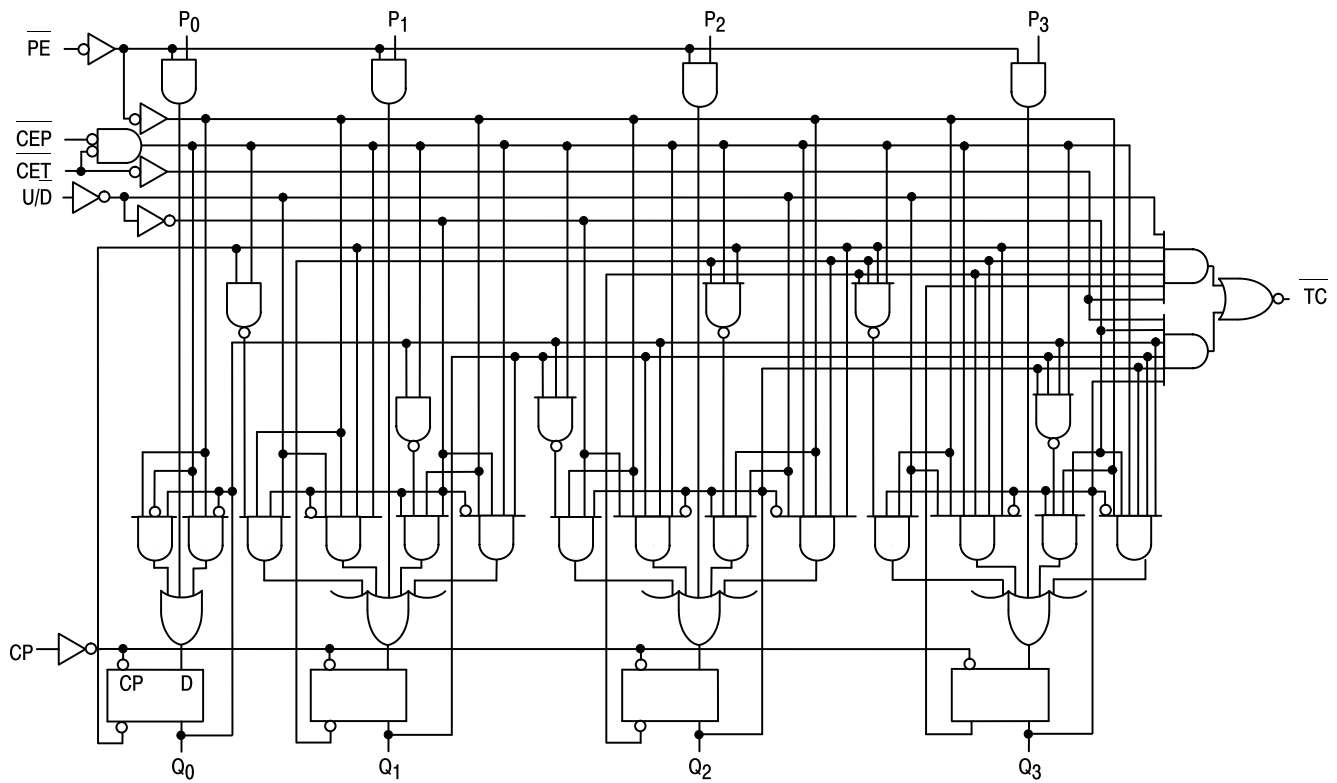
LOGIC DIAGRAMS

SN54/74LS168
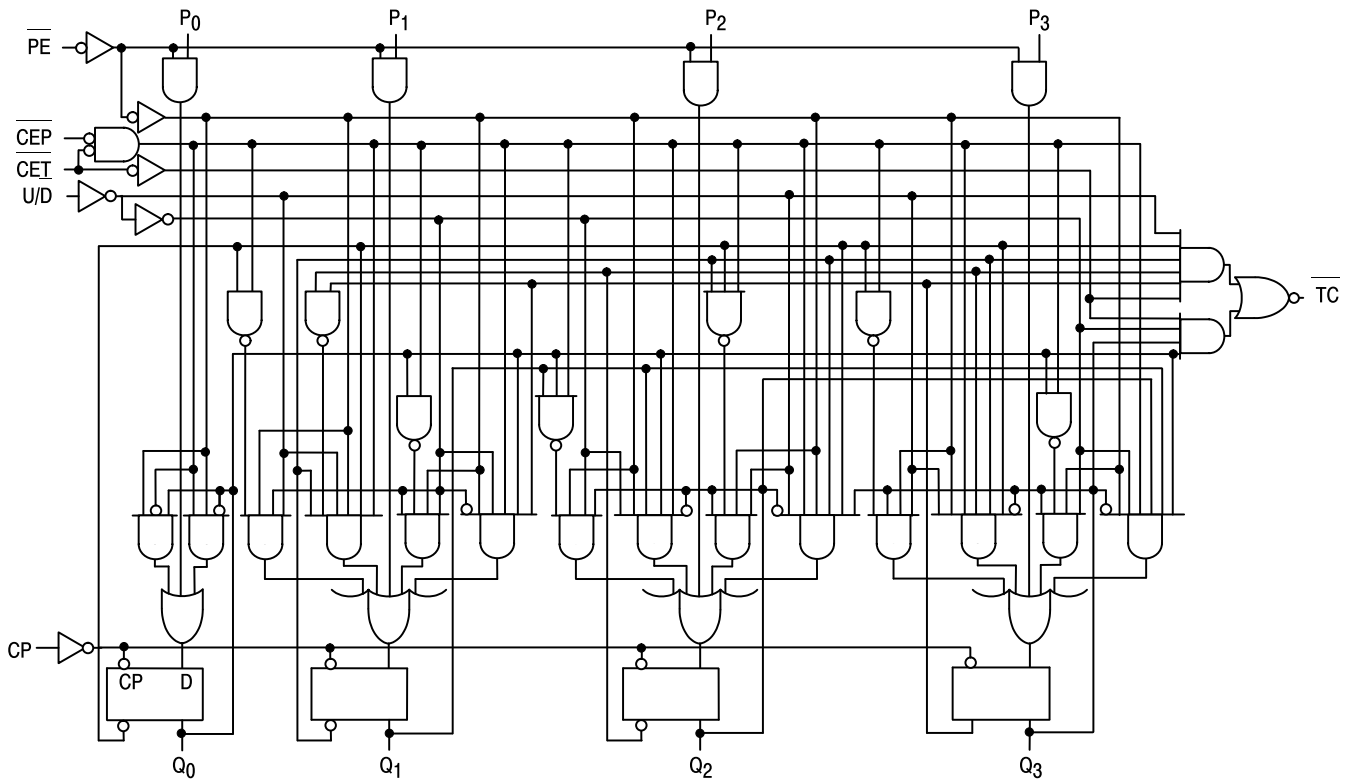
SN54/74LS168 • SN54/74LS169

LOGIC DIAGRAMS (continued)

SN54/74LS169

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54			4.0	mA
		74			8.0	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Other Inputs CET Input				20 40	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Other Input CET Input				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Other Input CET Input				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				34	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at one time, nor for more than 1 second.

FUNCTIONAL DESCRIPTION

The SN54/74LS168 and SN54/74LS169 use edge-triggered D-type flip-flops that have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter.

The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When PE is LOW, the data on the P_0–P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both CEP and CET must be LOW and PE must be HIGH. The U/D input then determines the direction of counting.

The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that CET is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 15 (9 for the SN54/74LS168) in the COUNT UP mode. The TC output state is not a function of the Count Enable Parallel (CEP) input level. The TC output of the SN54/74LS168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If illegal state occurs, the SN54/74LS168 will return to the legitimate sequence within two counts. Since the TC signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on TC. For this reason the use of TC as a clock signal is not recommended.

MODE SELECT TABLE

PE	CEP	CET	U/D	Action on Rising Clock Edge
L	X	X	X	Load (Pn → Qn)
H	L	L	H	Count Up (increment)
H	L	L	L	Count Down (decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SN54/74LS168 • SN54/74LS169

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f_{MAX}	Maximum Clock Frequency	25	32		MHz	
t_{PLH} t_{PHL}	Propagation Delay, Clock to TC		23 23	35 35	ns	
t_{PLH} t_{PHL}	Propagation Delay, Clock to any Q		13 15	20 23	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, CET to TC		15 15	20 20	ns	
t_{PLH} t_{PHL}	Propagation Delay, U/D to TC		17 19	25 29	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_W	Clock Pulse Width	25			ns	
t_S	Setup Time, Data or Enable	20			ns	
t_S	Setup Time PE	25			ns	V_{CC} = 5.0 V
t_S	Setup Time U/D	30			ns	
t_h	Hold Time Any Input	0			ns	

SN54/74LS168 • SN54/74LS169

AC WAVEFORMS
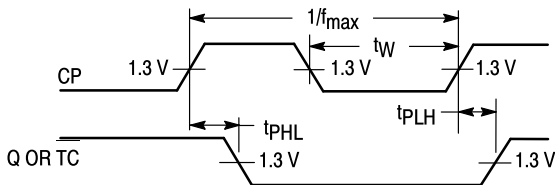
**Figure 1. Clock to Output Delays,
Count Frequency, and Clock Pulse Width**
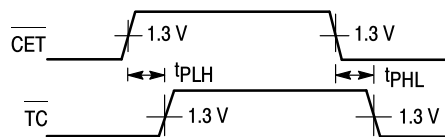
**Figure 2. Count Enable Trickle Input
To Terminal Count Output Delays**
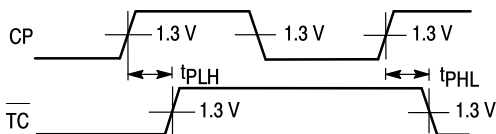
Figure 3. Clock to Terminal Delays
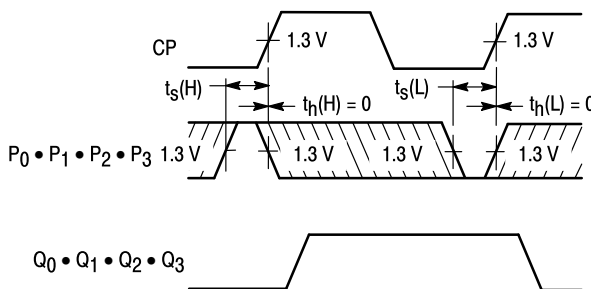
**Figure 4. Setup Time (t_S) and Hold (t_h)
for Parallel Data Inputs**
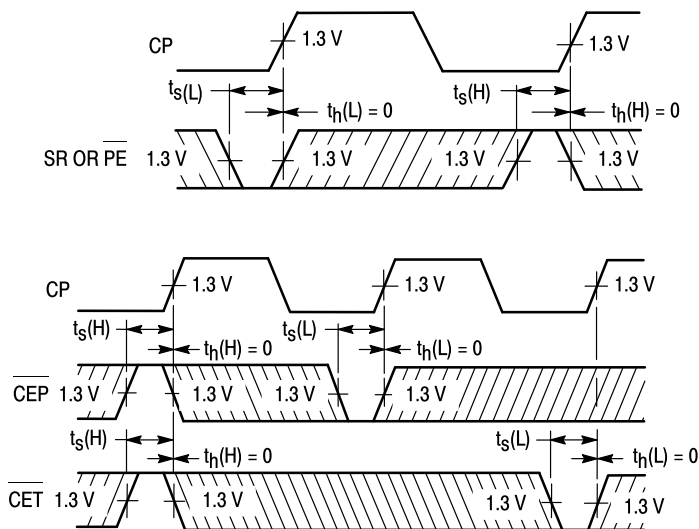
The shaded areas indicate when the
input is permitted to change for
predictable output performance.

**Figure 5. Setup Time and Hold Time for
Count Enable and Parallel Enable Inputs,
and Up-Down Control Inputs**
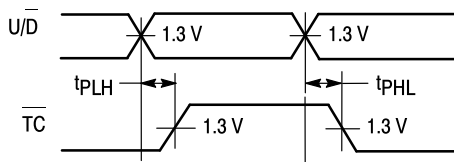
**Figure 6. Up-Down Input to
Terminal Count Output Delays**

Case 751B-03 D Suffix
16-Pin Plastic
SO-16
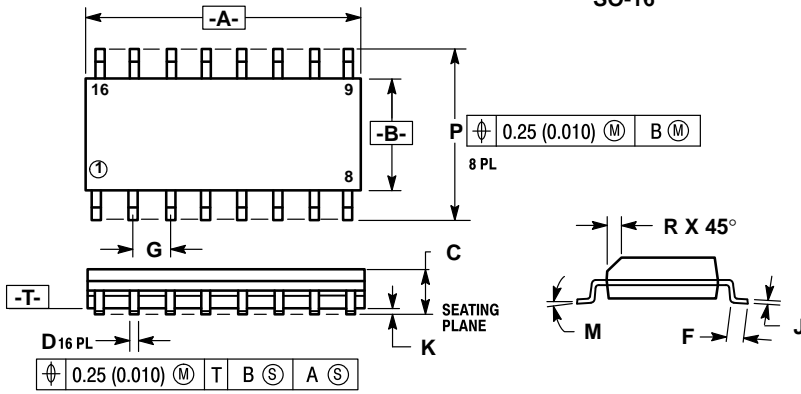
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Case 648-08 N Suffix
16-Pin Plastic
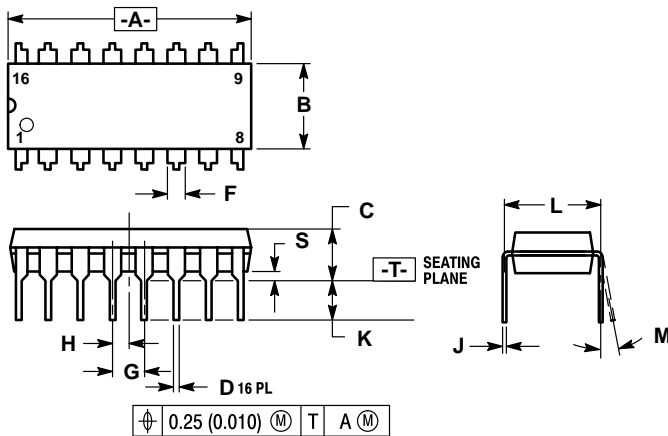
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

Case 620-09 J Suffix
16-Pin Ceramic Dual In-Line
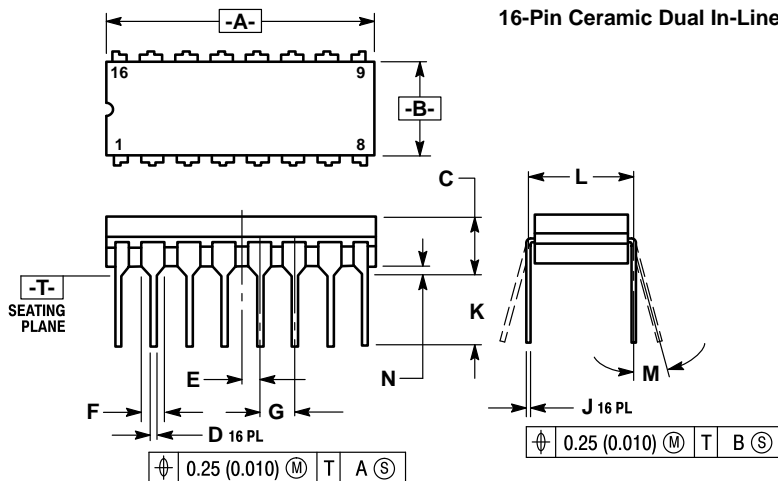
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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