2N4921 thru 2N4923 (SILICON)
MJE4921 thru MJE4923

MEDIUM-POWER PLASTIC NPN SILICON TRANSISTORS

. . . designed for driver circuits, switching, and amplifier applications. These high-performance plastic devices feature:

- Low Saturation Voltage – $V_{CE(sat)}$ = 0.6 Vdc (Max) @ I_C = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction – P_D = 30 and 40 W @ T_C = 25°C
- Excellent Safe Operating Area
- Gain Specified to I_C = 1.0 Amp
- Complement to PNP 2N4918, 2N4919, 2N4920 and MJE4918, MJE4919, MJE4920
- Choice of Packages – 2N4921 thru 2N4923, 30 Watts – Case 77
  MJE4921 thru MJE4923, 40 Watts – Case 199

3 AMPERE GENERAL PURPOSE POWER TRANSISTORS

40-80 VOLTS
30 and 40 WATTS

***MAXIMUM RATINGS**

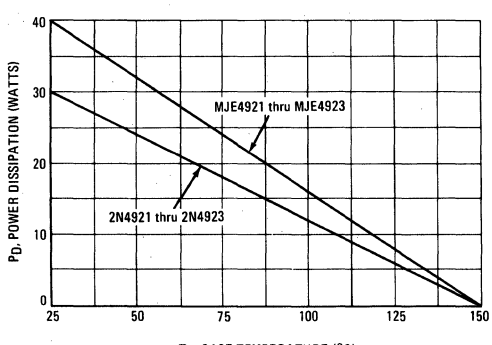
Rating	Symbol	2N4921 MJE4921	2N4922 MJE4922	2N4923 MJE4923	Unit
Collector-Emitter Voltage	V_{CEO}	40	60	80	Vdc
Collector-Base Voltage	V_{CB}	40	60	80	Vdc
Emitter-Base Voltage	V_{EB}	← 5.0 →			Vdc
Collector Current – Continuous (1)	I_C	← 1.0 →			Adc
		← 3.0 →			
Base Current – Continuous	I_B	← 1.0 →			Adc
		2N4921 Series		MJE4921 Series	
Total Device Dissipation @ T_C = 25°C	P_D	30		40	Watts
Derate above 25°C		0.24		0.32	W/°C
Operating & Storage Junction Temperature Range	T_J, T_{stg}	← -65 to +150 →			°C

THERMAL CHARACTERISTICS (2)

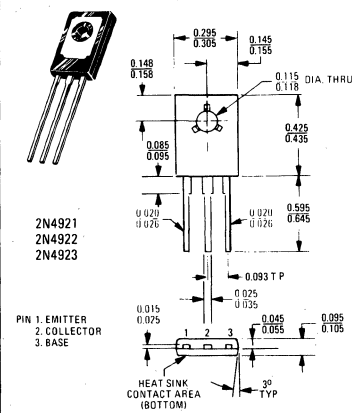
Characteristic	Symbol	2N4921/4923	MJE4921/4923	Unit
Thermal Resistance, Junction to Case	θ_{JC}	4.16	3.125	°C/W

(1) The 1.0 Amp maximum I_C value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current-handling capability of the device (see Figures 5 and 6).
(2) Recommend use of thermal compound for lowest thermal resistance.
*Indicates JEDEC Registered Data for 2N4921 Series.

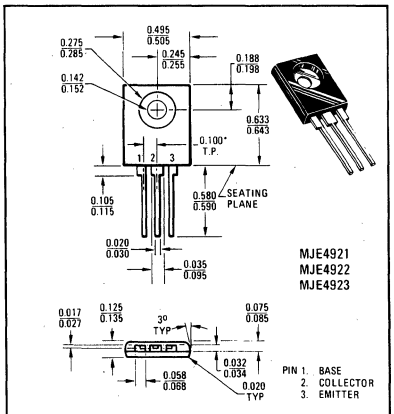
FIGURE 1 – POWER DERATING



Safe Area Curves are indicated by Figures 5 and 6. All limits are applicable and must be observed



Case 77-03
Style 1



Case 199-04
Style 1

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Figure No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1)		–	$V_{CEO(sus)}$			Vdc
(I_C = 0.1 Adc, I_B = 0)	2N4921, MJE4921			40	–	
	2N4922, MJE4922			60	–	
	2N4923, MJE4923			80	–	
Collector Cutoff Current		–	I_{CEO}			mAdc
(V_{CE} = 20 Vdc, I_B = 0)	2N4921, MJE4921			–	0.5	
(V_{CE} = 30 Vdc, I_B = 0)	2N4922, MJE4922			–	0.5	
(V_{CE} = 40 Vdc, I_B = 0)	2N4923, MJE4923			–	0.5	
Collector Cutoff Current		13	I_{CEX}			mAdc
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc)				–	0.1	
(V_{CE} = Rated V_{CEO}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 125°C)				–	0.5	
Collector Cutoff Current		–	I_{CBO}			mAdc
(V_{CB} = Rated V_{CB}, I_E = 0)				–	0.1	
Emitter Cutoff Current		–	I_{EBO}			mAdc
(V_{EB} = 5.0 Vdc, I_C = 0)				–	1.0	
ON CHARACTERISTICS						
DC Current Gain (1)		9	h_{FE}			–
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)				40	–	
(I_C = 500 mAdc, V_{CE} = 1.0 Vdc)				20	100	
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)				10	–	
Collector-Emitter Saturation Voltage (1)		10 12 14	$V_{CE(sat)}$	–	0.6	Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)						
Base-Emitter Saturation Voltage (1)		12 14	$V_{BE(sat)}$	–	1.3	Vdc
(I_C = 1.0 Adc, I_B = 0.1 Adc)						
Base-Emitter On Voltage (1)		12 14	$V_{BE(on)}$	–	1.3	Vdc
(I_C = 1.0 Adc, V_{CE} = 1.0 Vdc)						
SMALL-SIGNAL CHARACTERISTICS						
Current-Gain – Bandwidth Product		–	f_T			MHz
(I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 MHz)				3.0	–	
Output Capacitance		–	C_{ob}			pF
(V_{CB} = 10 Vdc, I_E = 0, f = 100 kHz)				–	100	
Small-Signal Current Gain		–	h_{fe}			–
(I_C = 250 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)				25	–	

(1) Pulse Test: PW≈300 μs, Duty Cycle≈2.0%.

*Indicates JEDEC Registered Data for 2N4921 Series.

FIGURE 2 – SWITCHING TIME EQUIVALENT CIRCUIT

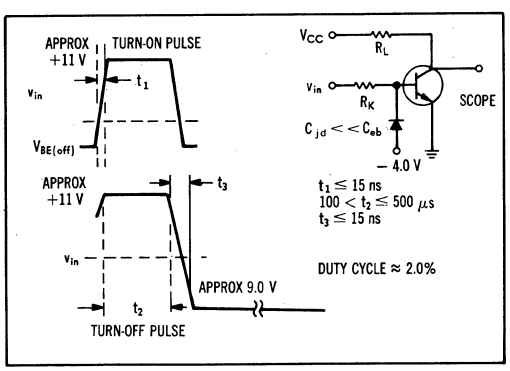


FIGURE 3 – TURN-ON TIME

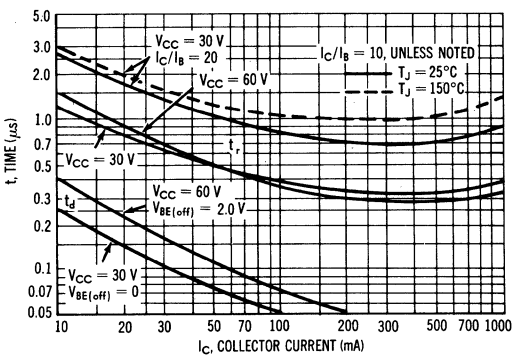
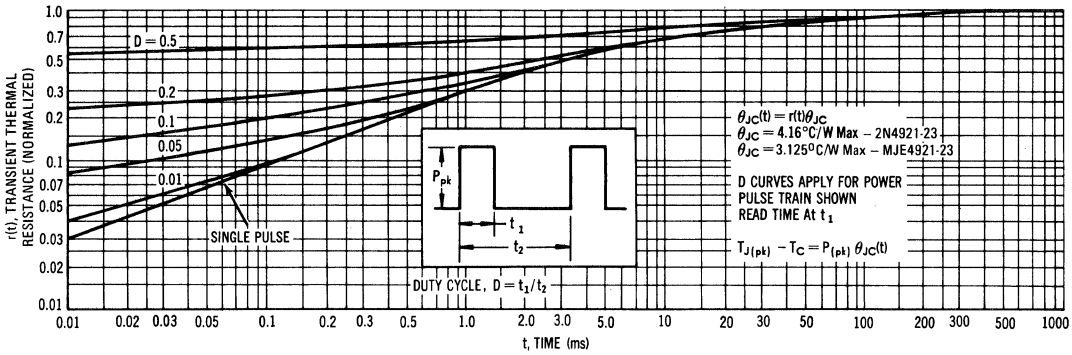


FIGURE 4 – THERMAL RESPONSE



ACTIVE – REGION SAFE OPERATING AREA

FIGURE 5 – 2N4921 thru 2N4923

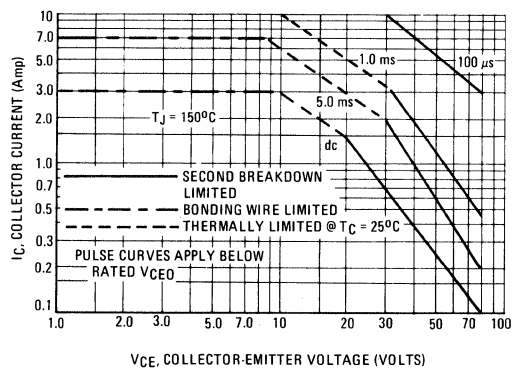
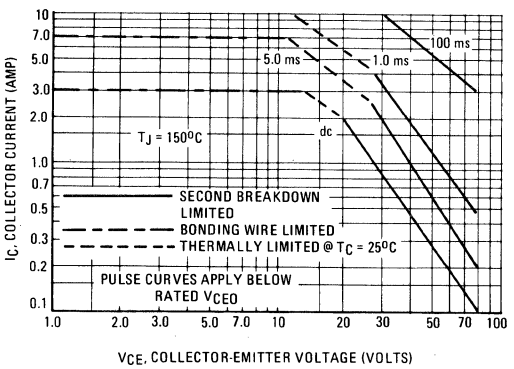


FIGURE 6 – MJE4921 thru MJE4923



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. (See AN-415)

FIGURE 7 – STORAGE TIME

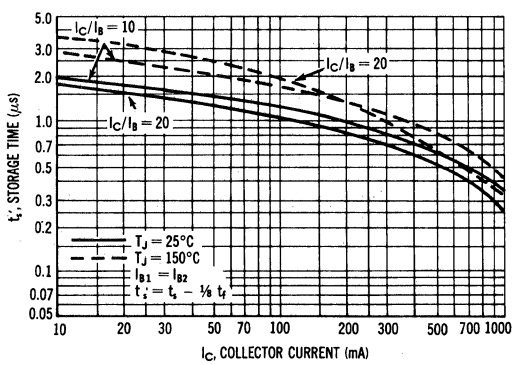


FIGURE 8 – FALL TIME

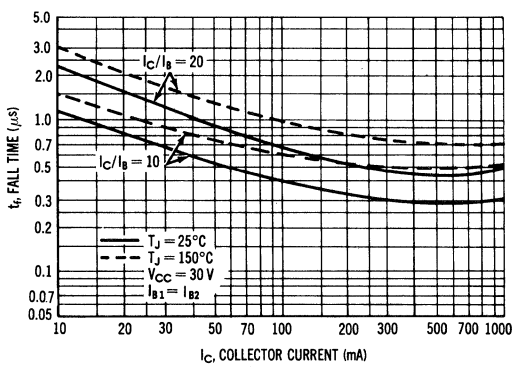


FIGURE 9 – CURRENT GAIN

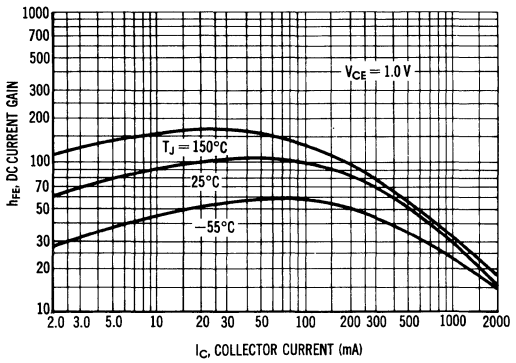


FIGURE 10 – COLLECTOR SATURATION REGION

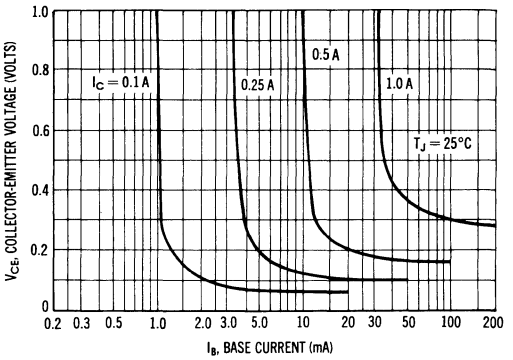


FIGURE 11 – EFFECTS OF BASE-EMITTER RESISTANCE

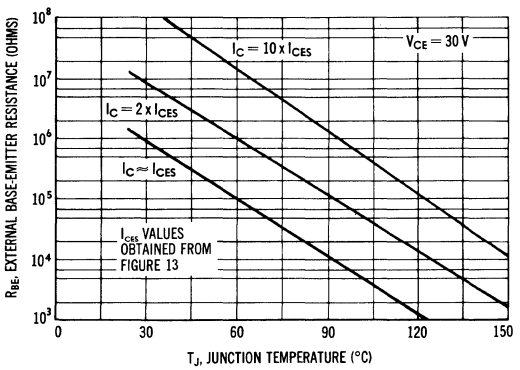


FIGURE 12 – "ON" VOLTAGE

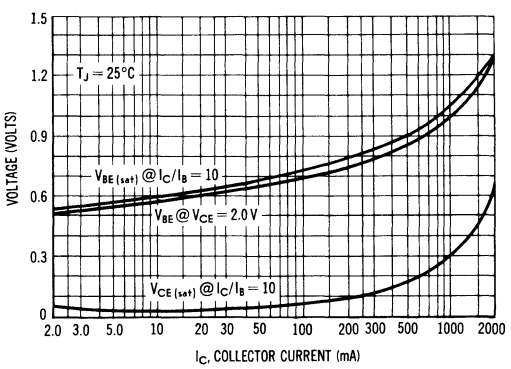


FIGURE 13 – COLLECTOR CUTOFF REGION

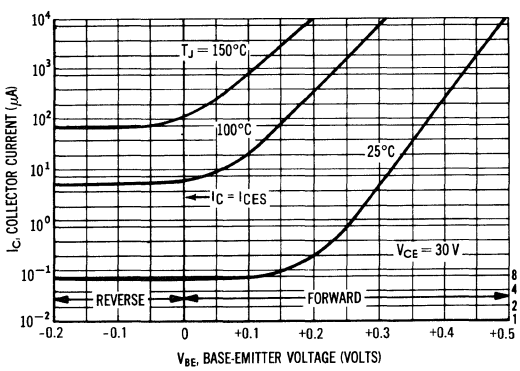


FIGURE 14 – TEMPERATURE COEFFICIENTS