MJ105 (SILICON)
BU105

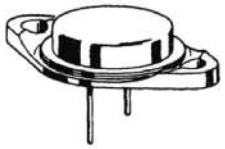
MOTOROLA

HORIZONTAL DEFLECTION SILICON TRANSISTORS

. . . designed for use in line operated black and white (19 and 20 inch 110° deflection circuits) or color (11 and 14 inch 90° deflection circuits) television receivers.

- High Collector-Emitter Voltage –
  V_{CER} (Peak) = 1400 Vdc – MJ105
  = 1500 Vdc – BU105
- Collector-Emitter Saturation Voltage –
  $V_{CE(sat)}$ = 5.0 Vdc (Max) @ I_C = 2.5 Adc
- Fall Time @ I_C = 2.0 Adc –
  t_f = 0.5 μs (Typ)
  = 1.0 μs (Max)

2.5 AMPERE
POWER TRANSISTORS
NPN SILICON
1400, 1500 VOLTS
10 WATTS



MAXIMUM RATINGS

Rating	Symbol	MJ105	BU105	Unit
Collector-Emitter Voltage	V_{CEO}	750		Vdc
Collector-Emitter Voltage – Continuous (R_{BE} = 100 Ω)	V_{CER}	750	750	V
Peak		1400	1500	
Collector-Base Voltage – Continuous	V_{CB}	750	750	V
Peak		1400	1500	
Emitter-Base Voltage	V_{EB}	5.0		Vdc
Collector Current – Continuous	I_C	2 5		Adc
Base Current – Positive	I_B	2 5		Adc
Negative		1 5		
Total Device Dissipation @ T_C = 90°C	P_D	10		Watts
Derate above 90°C		0.4		W/°C
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-65 to +115		°C

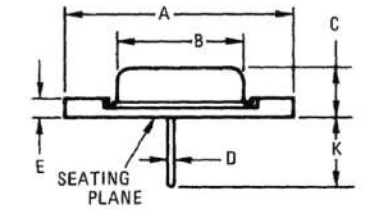
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	2 5	°C/W

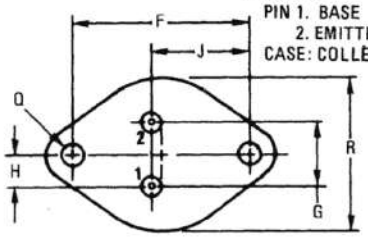
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector-Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)		$BV_{CEO(sus)}$	750	–	–	Vdc
Collector Cutoff Current		I_{CES}				mAdc
(V_{CE} = 1400 Vdc, V_{BE} = 0)	MJ105		–	–	1.0	
(V_{CE} = 1500 Vdc, V_{BE} = 0)	BU105		–	–	1 0	
Emitter-Base Voltage (I_E = 100 mAdc, I_C = 0)		BV_{EBO}	5.0	–	–	Vdc
ON CHARACTERISTICS						
Collector-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.5 Adc)		$V_{CE(sat)}$	–	–	5 0	Vdc
Base-Emitter Saturation Voltage (I_C = 2.5 Adc, I_B = 1.5 Adc)		$V_{BE(sat)}$	–	–	1.5	Vdc
DYNAMIC CHARACTERISTICS						
Current-Gain–Bandwidth Product (2) (I_C = 0 1 Adc, V_{CE} = 5.0 Vdc, f_{test} = 1.0 MHz)		f_T	–	7.5	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0 1 MHz)		C_{ob}	–	65	–	pF
SWITCHING CHARACTERISTICS (Figure 1 and text)						
Fall Time (I_C = 2.0 Adc, I_{B1} = 1.5 Adc, L_B = 12 μH, R_B = 2.5, Non-optimum values to comply with BU105 specification)		t_f	–	0 5	1.0	μs

(1) Pulse Test: Pulse Width 300 μs, Duty Cycle ≈ 2.0%.
(2) $f_T = |h_{fe}| \cdot f_{test}$



STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	7.62	0.250	0.300
D	0.99	1.09	0.039	0.043
E	–	3.43	–	0.135
F	29.90	30.40	1.177	1.197
G	10.67	11.18	0.420	0.440
H	5.33	5.59	0.210	0.220
J	16.64	17.15	0.655	0.675
K	11.18	12.19	0.440	0.480
Q	3.84	4.09	0.151	0.161
R	–	26.67	–	1.050

NOTE:
1. DIM "Q" IS DIA.

CASE 11

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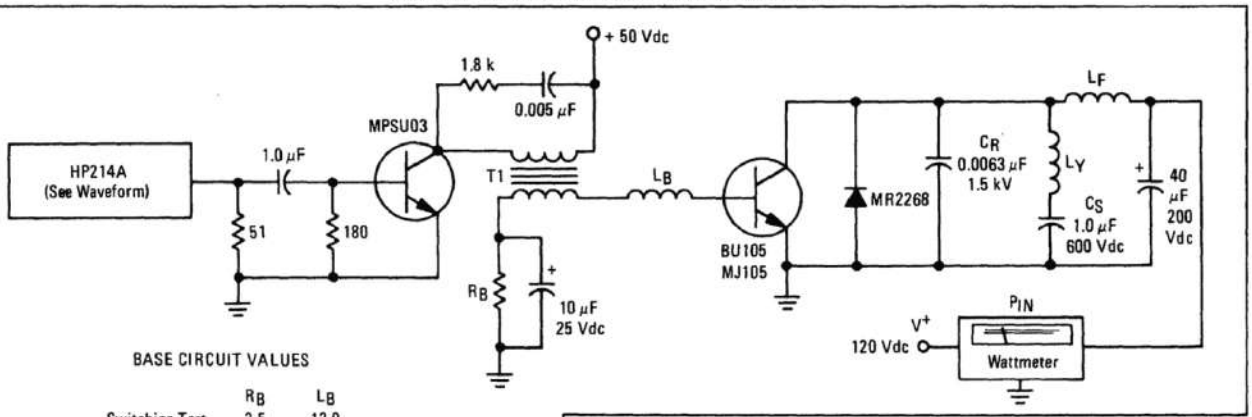
CIRCUIT OPTIMIZATION

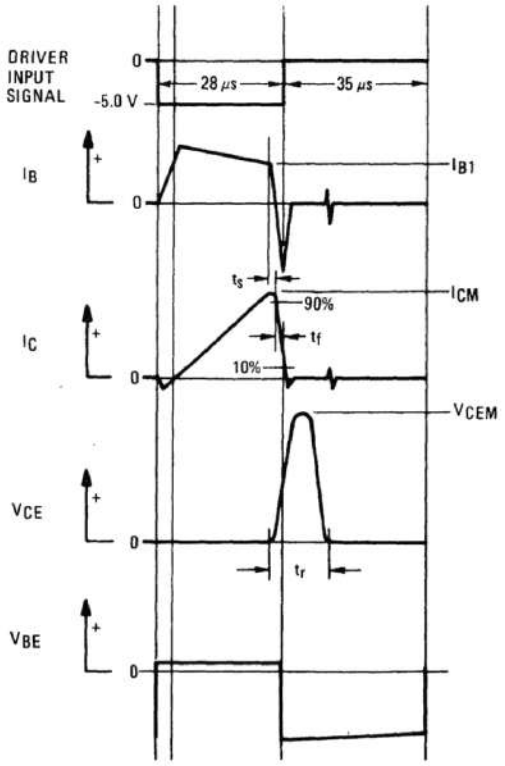
Test/application circuit and operating waveforms for BU105/MJ105 are shown in Figure 1. It may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, the circuit was designed with operating efficiency in mind, so that it could be used to evaluate devices by one simple criterion, supply power input. Excessive power input can be caused by a variety of problems, but it is the dissipation itself that is of fundamental importance. Once the transistor operating point has been established, fixed circuit values may be selected for the test fixture. Factory testing may then be made with one meter reading, without adjustment of the test apparatus.

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS



BASE CIRCUIT VALUES

	R_B	L_B
Switching Test	2.5	12.0
Optimum	7.0	15.0



FUNDAMENTAL WAVEFORMS OF A SIMPLIFIED HORIZONTAL DEFLECTION CIRCUIT

DESCRIPTION OF SPECIAL COMPONENTS

DUMMY YOKE INDUCTOR (L_Y)

2.0 mH, 52.5 turns, #16 AWG enamel wire 15 turns per layer, 3.5 layers on 1.375 inch diameter bobbin, enclosed in a Ferroxcube, cup core K535221-B2A, with a 0.687 inch diameter core, with 0.003 inch core gap. Use a nylon bolt and nut to hold cup halves together.

DUMMY HIGH VOLTAGE AND HORIZONTAL SCAN TRANSFORMER (L_F)

5.5 mH, 121 turns, #20 AWG enamel wire 33 turns per layer, 3.6 layers 1 mil mylar insulation between layers wound on 1 leg of Allen Bradley 0.5 inch square Ferrite "U" core (2) W03 material with 0.007 inch gap in each leg. Core halves held together with plastic.

DRIVER TRANSFORMER (T1)

Motorola part number 25D68782A05-1/4" laminate "E" iron core. Primary Inductance - 39 mH, Secondary Inductance - 0.22 mH, Leakage inductance with primary shorted - 2.0 μH. Primary 260 turns, #28 AWG enamel wire, Secondary 17 turns, #22 AWG enamel wire.

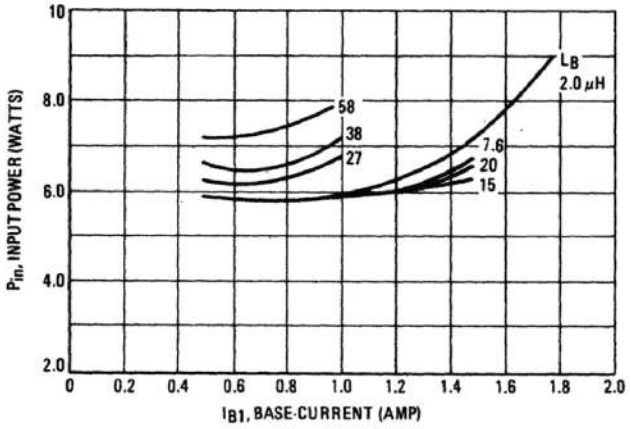
BASIC CONSIDERATIONS

The primary consideration when choosing a deflection transistor for a conventional (parallel connected) circuit, as shown in Figure 1, is one of voltage capability. The flyback voltage to which the device will be subjected is a relatively predictable value with respect to the main power supply voltage. This voltage pulse, shown in Figure 1, will usually be about 8 times the value of V^+, but may be varied somewhat by adjusting retrace time and flyback tuning. For this reason these high voltage devices are particularly useful in cost conscious solid state receivers, as they permit the use of an off-the-line half wave power supply.

COLLECTOR CIRCUIT VALUES

The power supply used in the circuit of Figure 1, was chosen to produce a 1000 volt collector pulse on the transistor, a conservative value, recommended for unregulated applications. The values of yoke (L_Y), flyback primary (L_F), retrace capacitor (C_R), and "S" shaping capacitor (C_S) shown, will result in a peak collector current of about 2.0 A. This is sufficient to deflect (and provide high voltage for) large screen 110° black and white or small 90° color receivers. Peak collector currents to 2.5 A may be handled by the BU105/MJ105. Holding the supply constant for most efficient application, adjustment of amount of deflection may be made by raising or lowering L_Y and L_F. Remember that $L_Y I_Y$ is constant for the fixed voltage situation, and actual deflection is proportional to $I_Y \sqrt{L_Y}$. Values of C_S and C_R must be varied inversely with L_Y to maintain retrace and "S" shaping periods.

FIGURE 2 – RELATIONSHIP OF POWER DISSIPATION TO L_B, WITH CHANGING I_{B1}, I_C = 2.0 A PEAK



BASE CIRCUIT VALUES

The driver power supply and driver transistor type can be selected according to convenience. A TO-5 or Uniwatt type will generally be needed. Once this is done, the turns ratio of the driver transformer can be picked to produce about 4 to 5 volts peak to peak at the base of the output device. Tight coupling between windings is recommended on early designs to allow optimizing leakage inductance by adding inductance externally. Later, the leakage can be "designed in" to the transformer. The R_B and its bypass electrolytic, often called the "speed up" circuit, allows adjustment of I_{B1} (or I_B "end of scan" or I_B end) while still providing a low ac impedance for good turn-off of the output device. In Figure 2, the effects of varying L_B and I_{B1} on the total power input to the deflection circuit are shown. Note that an optimum L_B can be found which will produce low dissipation over a wide range of I_{B1}. This is desirable in order to produce efficient operation over a wide range of circuit component tolerances. Likewise, best L_B also gives the least sensitivity to output transistor h_{FE}.

The best value of L_B found in Figure 2 is 15 μH. Remember that this is the sum of the actual leakage inductance of the transformer (secondary inductance with primary shorted) and an external L, if necessary. The best value of I_{B1} is 0.8 A achieved in the typical device by using R_B = 7 Ω, derived experimentally.

These are the choices recommended for the test fixture, when the transistor is used at I_{CM} = 2.0 A. For other values of I_{CM} the drive circuit components must be changed. Figure 3 shows the values of L_B and I_{B1} which should be used.

The value of R_B which will be required to produce the I_{B1} is also given, but of course, it is not an independent variable.

PERFORMANCE

Shown in Figures 4 and 5 are the results which will be typically obtained with the test circuit at various operating conditions.

FIGURE 3 – INTERRELATION OF R_B, L_B, AND I_{B1}

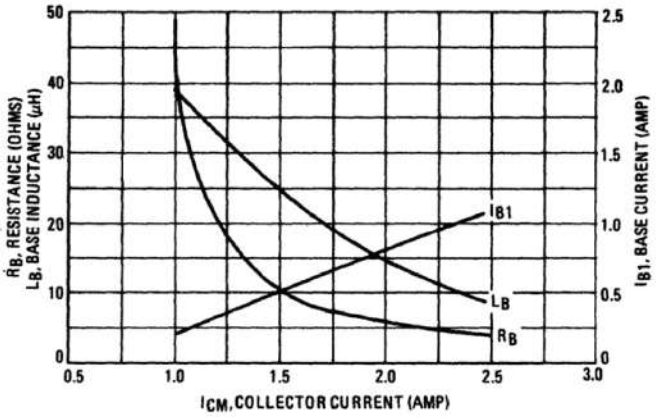


FIGURE 4 – INTERRELATION OF t_f, FALL TIME AND t_s, STORAGE TIME

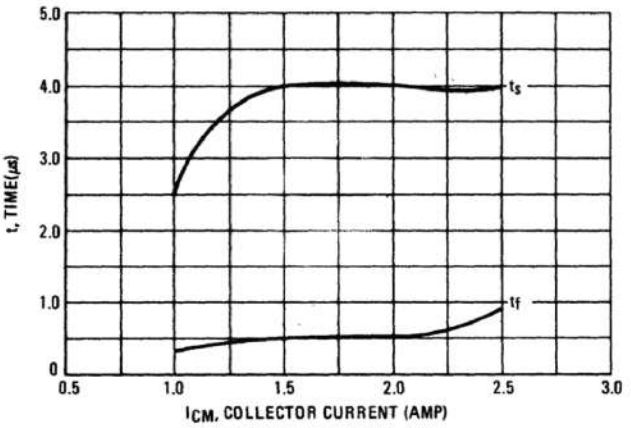
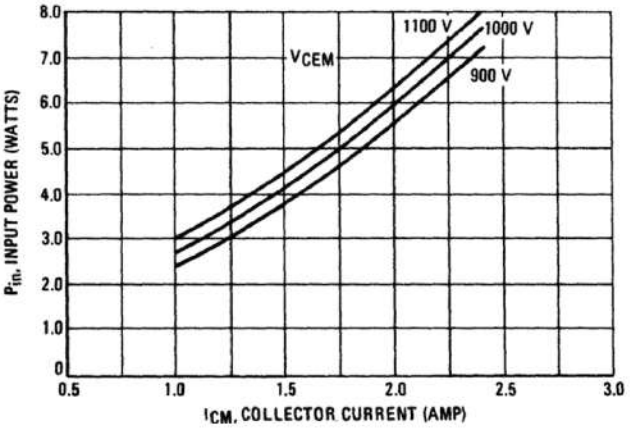


FIGURE 5 – P_{IN}, POWER DISSIPATION, WITH DEVIATIONS OF V_{CEM} AND I_{CM}



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TYPICAL TRANSISTOR CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

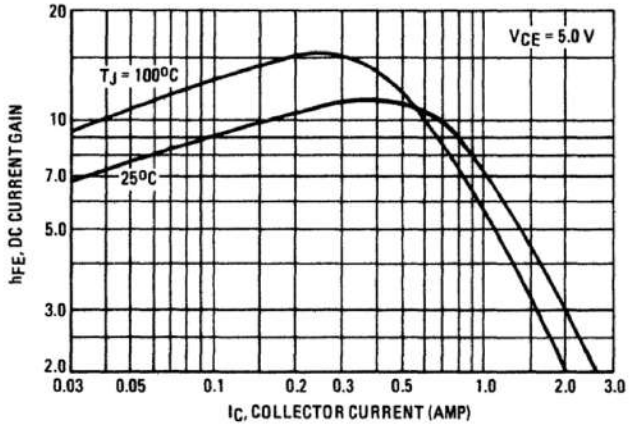

FIGURE 2 – "ON" VOLTAGES

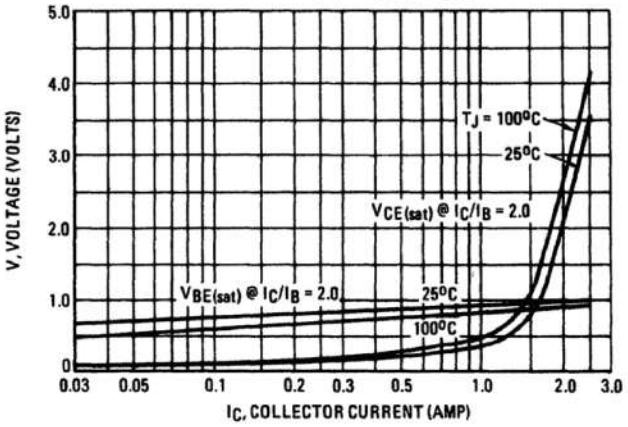

FIGURE 3 – SAFE OPERATING AREA

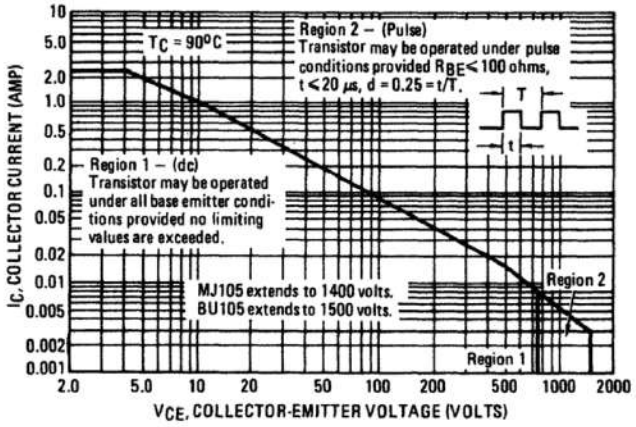

FIGURE 4 – COLLECTOR CUTOFF CURRENT