

DATA SHEET

BUT18F; BUT18AF
Silicon diffused power transistors

Product specification
Supersedes data of 1997 Aug 13

1999 Jun 11

Silicon diffused power transistors**BUT18F; BUT18AF****DESCRIPTION**

High-voltage, high-speed, glass-passivated NPN power transistor in a SOT186 package with electrically isolated mounting base.

APPLICATIONS

- Converters
- Inverters
- Switching regulators
- Motor control systems.

PINNING

PIN	DESCRIPTION
1	base
2	collector
3	emitter
mb	mounting base; electrically isolated from all pins

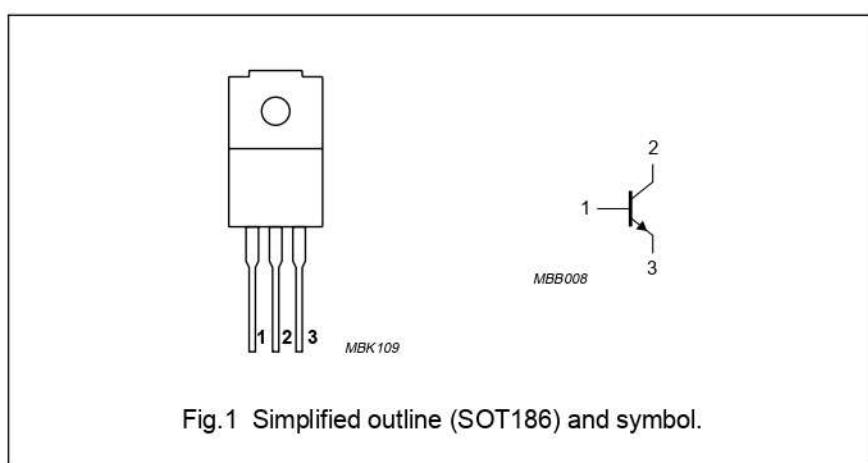


Fig.1 Simplified outline (SOT186) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{CESM}	collector-emitter peak voltage BUT18F BUT18AF	$V_{BE} = 0$	850 1000	V V
V_{CEO}	collector-emitter voltage BUT18F BUT18AF	open base	400 450	V V
V_{CEsat}	collector-emitter saturation voltage	see Fig.7	1.5	V
I_{Csat}	collector saturation current		4	A
I_C	collector current (DC)	see Fig.4	6	A
I_{CM}	collector current (peak value)	see Fig.4	12	A
P_{tot}	total power dissipation	$T_h \leq 25^\circ\text{C}$; see Fig.2	33	W
t_f	fall time	resistive load; see Figs 10 and 11	0.8	μs

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R_{thj-h}	thermal resistance from junction to external heatsink	note 1	6.15	K/W
		note 2	3.65	K/W

Notes

1. Mounted **without** heatsink compound and 30 ± 5 N force on centre of package.
2. Mounted **with** heatsink compound and 30 ± 5 N force on centre of package.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CESM}	collector-emitter peak voltage BUT18F BUT18AF	$V_{BE} = 0$	-	850 1000	V V
V_{CEO}	collector-emitter voltage BUT18F BUT18AF	open base	-	400 450	V V
I_{Csat}	collector saturation current		-	4	A
I_C	collector current (DC)	see Fig.4	-	6	A
I_{CM}	collector current (peak value)	see Fig.4	-	12	A
I_B	base current (DC)		-	3	A
I_{BM}	base current (peak value)		-	6	A
P_{tot}	total power dissipation	$T_h \leq 25^\circ\text{C}$; see Fig.2; note 1	-	20	W
		$T_h \leq 25^\circ\text{C}$; see Fig.2; note 2	-	33	W
T_{stg}	storage temperature		-65	+150	$^\circ\text{C}$
T_j	junction temperature		-	150	$^\circ\text{C}$

Notes

1. Without heatsink compound.
2. With heatsink compound.

ISOLATION CHARACTERISTICS

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{isolM}	isolation voltage from all terminals to external heatsink (peak value)	-	1500	V
C_{isol}	isolation capacitance from collector to external heatsink	12	-	pF

CHARACTERISTICS $T_j = 25^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CEO}sust$	collector-emitter sustaining voltage BUT18F BUT18AF	$I_C = 100 \text{ mA}; I_{Boff} = 0;$ $L = 25 \text{ mH}$; see Figs 3 and 6	400 450	- -	- -	V V
V_{CEsat}	collector-emitter saturation voltage	$I_C = 4 \text{ A}; I_B = 800 \text{ mA}$; see Fig.7	-	-	1.5	V
V_{BEsat}	base-emitter saturation voltage	$I_C = 4 \text{ A}; I_B = 800 \text{ mA}$; see Fig.8	-	-	1.3	V
I_{CES}	collector-emitter cut-off current	$V_{CE} = V_{CESMmax}; V_{BE} = 0;$ note 1	-	-	1	mA
		$V_{CE} = V_{CESMmax}; V_{BE} = 0;$ $T_j = 125^\circ\text{C}$; note 1	-	-	2	mA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 9 \text{ V}; I_C = 0$	-	-	10	mA

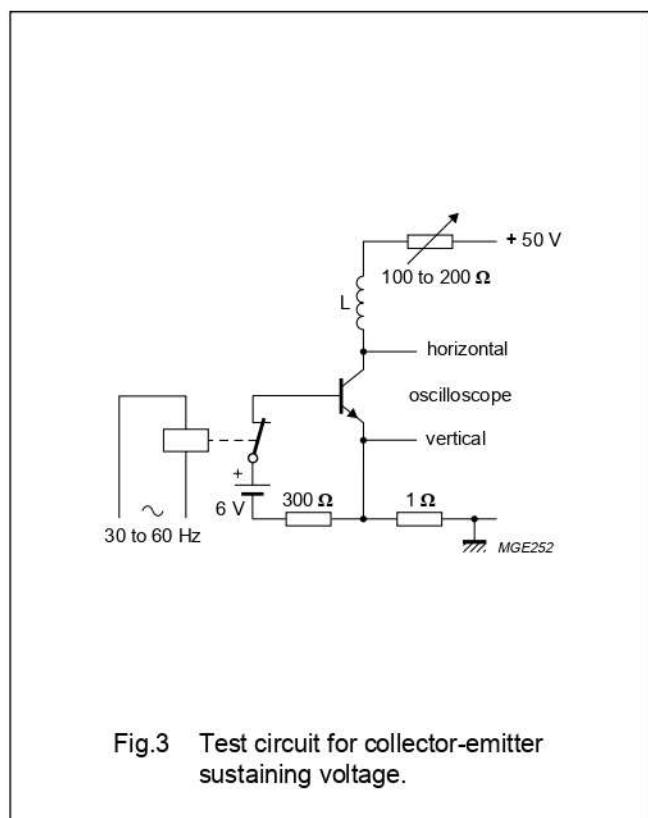
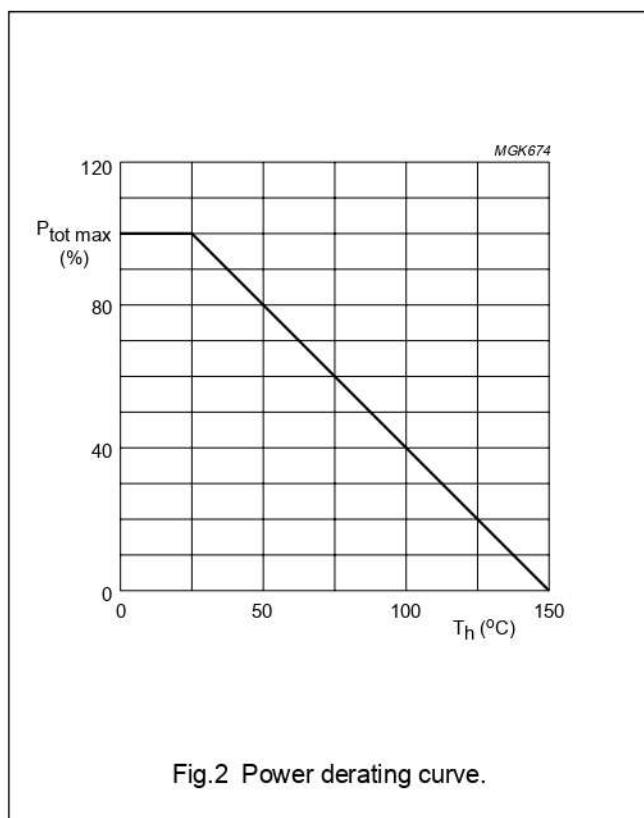
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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
h_{FE}	DC current gain	$V_{CE} = 5 \text{ V}; I_C = 10 \text{ mA};$ see Fig.9	10	18	35	
		$V_{CE} = 5 \text{ V}; I_C = 1 \text{ A};$ see Fig.9	10	20	35	
Switching times resistive load (see Figs 10 and 11)						
t_{on}	turn-on time	$I_{Con} = 4 \text{ A};$ $I_{Bon} = -I_{Boff} = 800 \text{ mA}$	-	-	1	μs
t_s	storage time	$I_{Con} = 4 \text{ A};$ $I_{Bon} = -I_{Boff} = 800 \text{ mA}$	-	-	4	μs
t_f	fall time	$I_{Con} = 4 \text{ A};$ $I_{Bon} = -I_{Boff} = 800 \text{ mA}$	-	-	0.8	μs
Switching times inductive load (see Figs 10 and 13)						
t_s	storage time	$I_{Con} = 4 \text{ A}; I_{Bon} = 800 \text{ mA}$	-	1.6	2.5	μs
t_f	fall time	$I_{Con} = 4 \text{ A}; I_{Bon} = 800 \text{ mA}$	-	150	400	ns

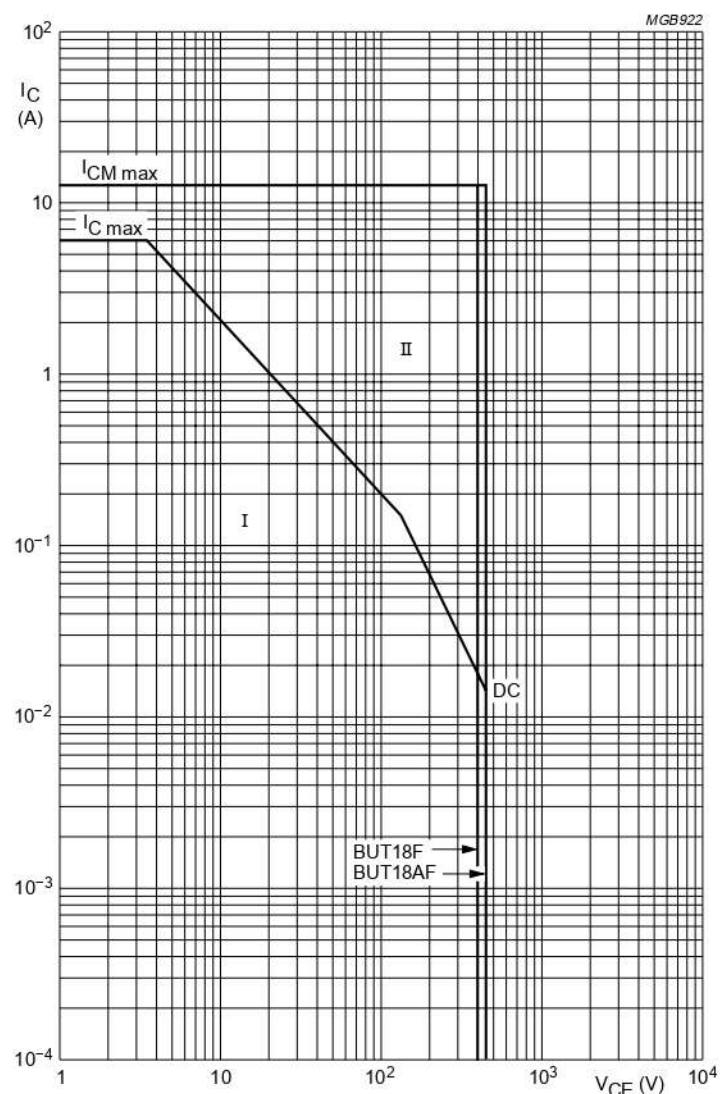
Note

1. Measured with a half-sinewave voltage (curve tracer).



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Mounted **without** heatsink compound and 30 ± 5 N force on centre of package.

$T_{mb} < 25^\circ\text{C}$

I - Region of permissible DC operation.

II - Permissible extension for repetitive pulse operation.

Fig.4 Forward bias SOAR.

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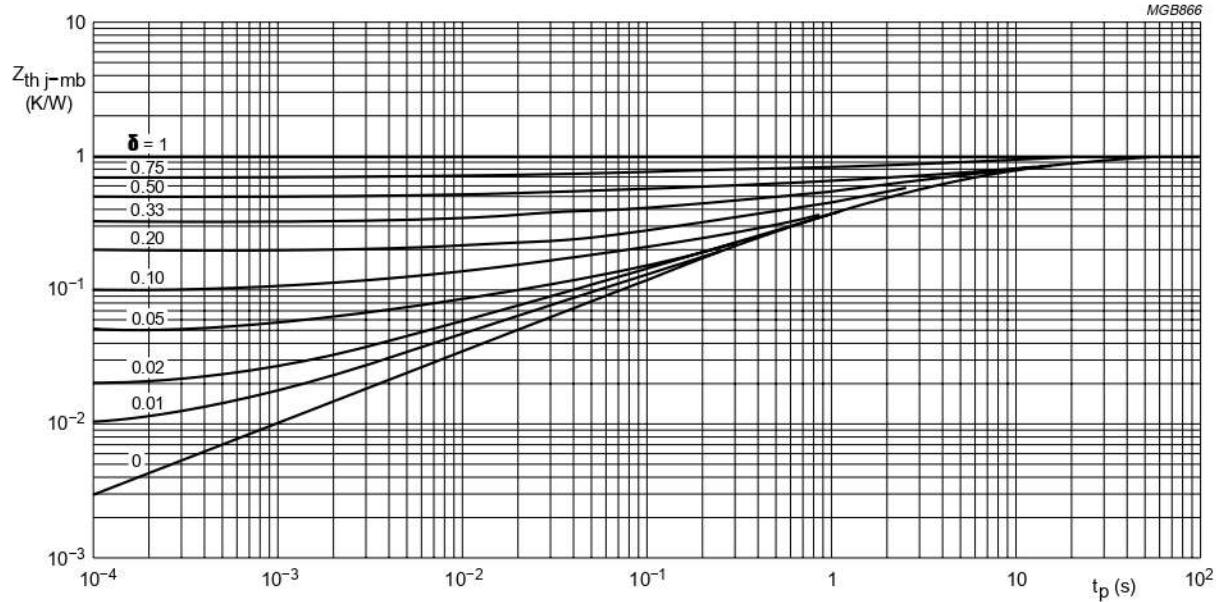


Fig.5 Transient thermal impedance.

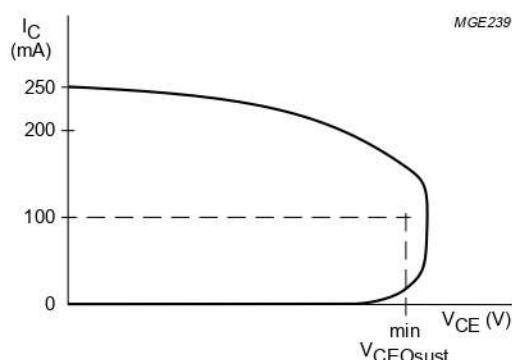


Fig.6 Oscilloscope display for collector-emitter sustaining voltage.

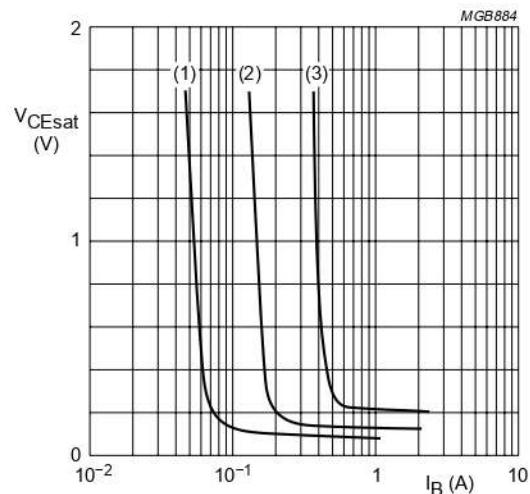
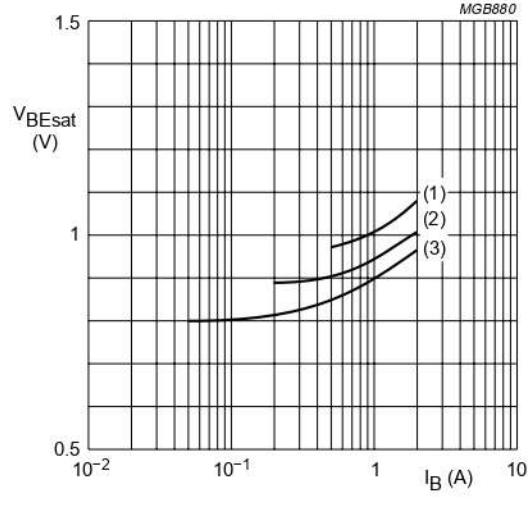


Fig.7 Collector-emitter saturation voltage as a function of base current.

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 $T_j = 25^\circ\text{C}$.

- (1) $I_C = 4\text{ A}$.
- (2) $I_C = 2\text{ A}$.
- (3) $I_C = 1\text{ A}$.

Fig.8 Base-emitter saturation voltage as a function of base current.

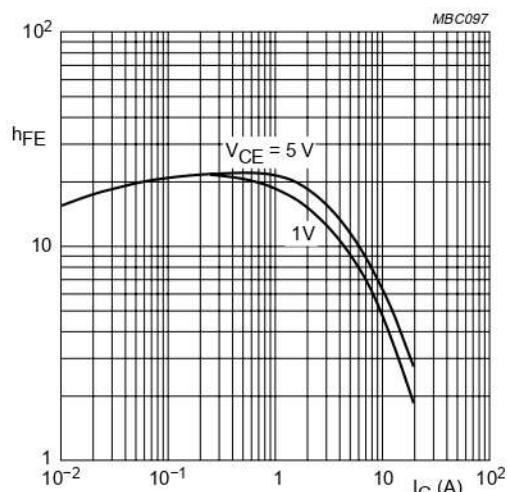
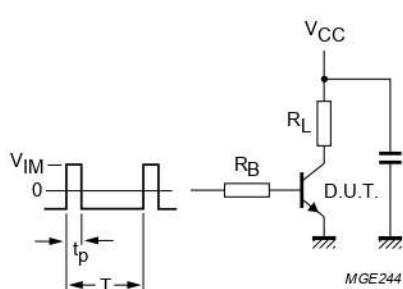
 $V_{CE} = 5\text{ V}; T_j = 25^\circ\text{C}$.

Fig.9 DC current gain; typical values.



$V_{CC} = 250\text{ V}$; $t_p = 20\text{ }\mu\text{s}$; $V_{IM} = -6$ to $+8\text{ V}$; $t_p/T = 0.01$.
The values of R_B and R_L are selected in accordance with I_{Con} and I_{Bon} requirements.

Fig.10 Test circuit resistive load.

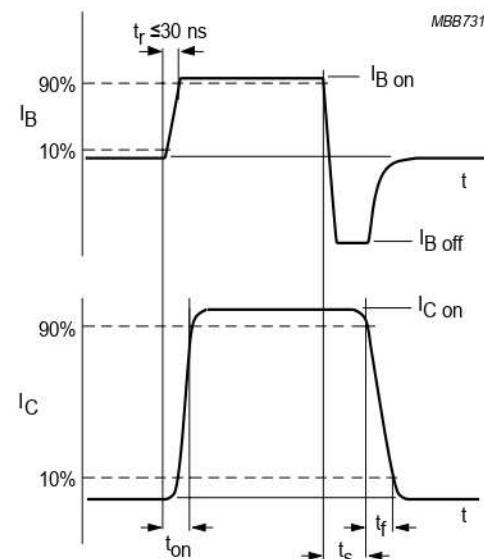
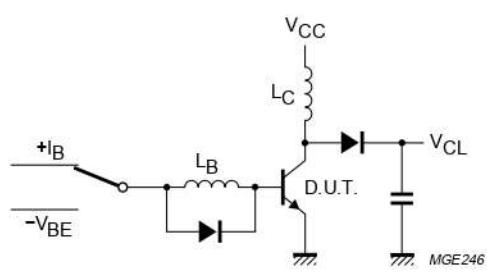
 $t_r \leq 20\text{ ns}$.

Fig.11 Switching times waveforms with resistive load.

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$V_{CL} = 300 \text{ V}$; $V_{CC} = 30 \text{ V}$; $V_{BE} = -5 \text{ V}$; $L_B = 1 \mu\text{H}$; $L_C = 200 \mu\text{H}$.

Fig.12 Test circuit inductive load.

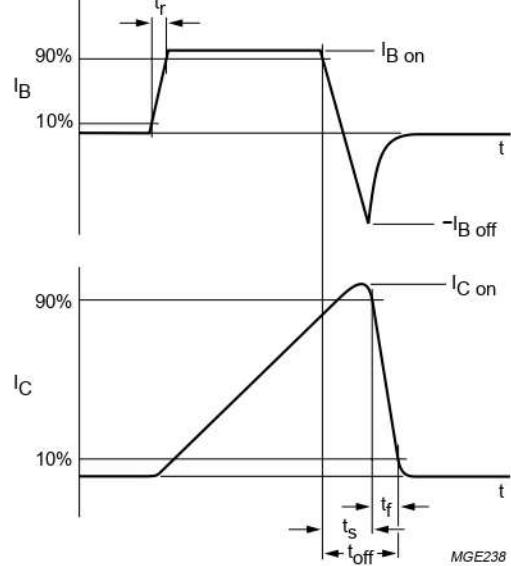


Fig.13 Switching time waveforms with inductive load.

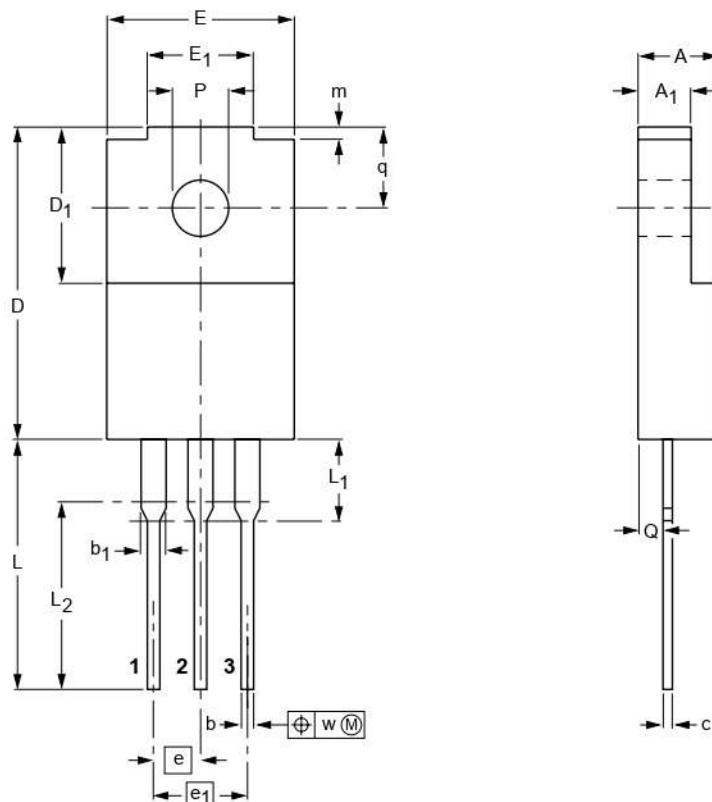
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PACKAGE OUTLINE

Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3 lead TO-220 exposed tabs

SOT186



0 5 10 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	c	D	D ₁	E	E ₁	e	e ₁	L	L ₁ ⁽¹⁾	L ₂	m	P	Q	q	w
mm	4.4	2.9	0.9	1.5	0.55	17.0	7.9	10.2	5.7	2.54	5.08	14.3	4.8	10	0.9	3.2	1.4	4.4	0.4
	4.0	2.5	0.7	1.3	0.38	16.4	7.5	9.6	5.3			13.5	4.0		0.5	3.0	1.2	4.0	0.4

Note

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT186		TO-220				97-06-11

Silicon diffused power transistors**BUT18F; BUT18AF****DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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